Open Hardware 2016 Design Contest

Please check the rules on the Open Hardware website:

http://www.openhw.eu/rules.html

For any clarification, please contact XUP xup@xilinx.com.

Deadline

You must upload an archive which will include your project files, and documentation, to the competition upload server by 30th June 2016. Upload instructions will be provided to your team separately.

Project requirements

You must use the Xilinx Vivado software (preferably 2015.4). Entries based on ISE will not be accepted. You must use a Xilinx series 7 device or later (Zynq, Artix, Kintex, Virtex 7).

Entry requirements

You must upload your entry as a compressed archive (.zip or tar.gz), and the archive size should be <100MB. You should try to upload your full, precompiled project, and you must include the bitstream. Please contact XUP if you have difficulties uploading your entry, or if file size is a problem.

Your archive should include:

- Full Vivado Project directories (including SDK or HLS projects if applicable).
- All custom IP that you use in your design, preferably saved in a top level directory called “ip”
- A readme file with information about your team, project description, instructions to test your design, and a link to your YouTube video. A template readme.txt file will be provided.
- Project report (pdf format)

Your uploaded archive must use this file naming convention:

<category>_<team number>_<supervisor surname>_< date>_<version>.zip or .tar.gz

Where category is < emb_student|fpga_student| emb_phd|fpga_phd>

Date is <YYYYMMDD>

Version should be the number of the uploaded archive, starting at 1.

e.g. emb_phd_XIL-00001_mccabe_20160630_1.zip

You can upload updated versions of your project (each <100MB). You should try to minimize the number of versions you upload. If you upload a later version of your project, please contact XUP to request the removal of your earlier version.

Upload instructions

You will be provided with details on the upload server, and how to upload your archive later.

Video

As part of your entry, you must upload a video to YouTube (maximum 2 minutes), giving a brief description and overview of your project, and showing your design running in hardware. If you have a problem uploading videos to YouTube, please contact XUP.

Along with the 2 minute video, you can also upload a longer video to YouTube.

All videos uploaded to YouTube should include the "Xilinx XUP OpenHardware2016"+ <Team Number> at the end video title to make the video easily searchable.

You should not include a copy of your video inside your project archive, but you must include a link to the video in a readme.txt file in the top level of your archive.

Example videos from 2015 can be found here:

http://www.openhw.eu/2015-finalists.html

Criteria for Judging

Projects will be judged equally across all of the following categories:

- Innovation (20%)
- Design Complexity (20%)
- Implementation (20%) - Demonstrate the design functioning correctly in hardware
- Documentation/Report (20%) - Project report and documentation (including source code documentation)
- Reusability (20%) – Well-defined and documented IP, and well-structured projects that facilitate reuse. You are encouraged to package and use all of your custom IP using the IP packager, and to use a Vivado IP Integrator Block Design for your project.
  Marks will also be given for IP or projects that you have shared or can commit to share with the community after the competition.
  In your project report, please detail any plans you have to share all or parts of your project.